











CSD17579Q3A

SLPS527-SEPTEMBER 2014

CSD17579Q3A 30 V N-Channel NexFET™ Power MOSFETs

Features

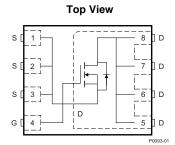
- Low Q_a and Q_{ad}
- Low R_{DS(on)}
- Low Thermal Resistance
- Avalanche Rated
- Pb-Free
- **RoHS Compliant**
- Halogen Free
- SON 3.3 mm × 3.3 mm Plastic Package

Applications

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom, and Computing Systems
- Optimized for Control FET Applications

3 Description

This 30 V, 8.7 m Ω , SON 3.3 mm × 3.3 mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



R_{DS(on)} vs V_{GS} 30 $T_C = 25^{\circ}C$, $I_D = 8 A$ $T_C = 125^{\circ}C$, $I_D = 8 A$ 27 $R_{DS(on)}$ - On-State Resistance (m Ω) 24 21 18 15 12 9 6 8 10 12 0 V_{GS} - Gate-to-Source Voltage (V)

Product Summary

$T_A = 25^\circ$	С	TYPICAL VA	UNIT		
V_{DS}	Drain-to-Source Voltage	30		V	
Q_g	Gate Charge Total (4.5 V) 5.3				
Q_{gd}	Gate Charge Gate-to-Drain	1.2	nC		
D	Drain-to-Source On-Resistance	V _{GS} = 4.5 V	11.8	mΩ	
R _{DS(on)}	Drain-to-Source On-Resistance	V _{GS} = 10 V	8.7	mΩ	
V _{GS(th)}	Threshold Voltage	1.5	٧		

Ordering Information⁽¹⁾

Device	Media	Qty	Package	Ship
CSD17579Q3A	13-Inch Reel	2500	SON 3.3 x 3.3 mm	Tape and
CSD17579Q3AT	7-Inch Reel	250	Plastic Package	Reel

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T _A = 2	5°C	VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	±20	V
	Continuous Drain Current (Package limited)	20	
I _D	Continuous Drain Current (Silicon limited), $T_C = 25$ °C	39	Α
	Continuous Drain Current ⁽¹⁾	11	
I _{DM}	Pulsed Drain Current ⁽²⁾	106	Α
n	Power Dissipation ⁽¹⁾	3.2	W
P _D	Power Dissipation, T _C = 25°C	29	VV
T _J , T _{stg}	Operating Junction and Storage Temperature Range	-55 to 150	ů
E _{AS}	Avalanche Energy, single pulse I_D = 17 A, L = 0.1 mH, R_G = 25 Ω	14	mJ

- (1) Typical $R_{\theta JA} = 50^{\circ} \text{C/W}$ on a 1-inch², 2-oz. Cu pad on a 0.06inch thick FR4 PCB.
- (2) Max $R_{\theta JC} = 5.4$ °C/W, pulse duration ≤ 100 µs, duty cycle $\leq 1\%$

Gate Charge

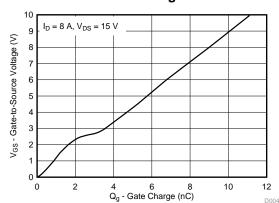






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4 Revision History

DATE	REVISION	NOTES
September 2014	*	Initial release.

5 Specifications

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5.1 Electrical Characteristics

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

(1 _A – 20	C unless otherwise stated)					
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC (CHARACTERISTICS					
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V
I_{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = 24 V			1	μΑ
I_{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.1	1.5	1.9	V
Б	Drain-to-Source On-Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 8 \text{ A}$		11.8	14.2	mΩ
R _{DS(on)}	Drain-to-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 8 \text{ A}$		8.7	10.2	mΩ
g_{fs}	Transconductance	$V_{DS} = 3 \text{ V}, I_{D} = 8 \text{ A}$		37		S
DYNAMIC	C CHARACTERISTICS		·			
C _{iss}	Input Capacitance			768	998	pF
C _{oss}	Output Capacitance	$V_{GS} = 0 \text{ V}, V_{DS} = 15 \text{ V}, f = 1 \text{ MHz}$		93	121	pF
C _{rss}	Reverse Transfer Capacitance			38	49	pF
R _G	Series Gate Resistance			1.9	3.8	Ω
Qg	Gate Charge Total (4.5 V)			5.3	6.9	
Qg	Gate Charge Total (10 V)			11.5	15.0	nC
Q _{gd}	Gate Charge Gate-to-Drain	V _{DS} = 15 V, I _D = 8 A		1.2		nC
Q _{gs}	Gate Charge Gate-to-Source			2.2		nC
Q _{g(th)}	Gate Charge at V _{th}			1.1		nC
Q _{oss}	Output Charge	V _{DS} = 15 V, V _{GS} = 0 V		3.0		nC
t _{d(on)}	Turn On Delay Time			2		ns
t _r	Rise Time	V _{DS} = 15 V, V _{GS} = 10 V,		5		ns
t _{d(off)}	Turn Off Delay Time	$I_{DS} = 8 \text{ A}, R_G = 0 \Omega$		11		ns
t _f	Fall Time			1		ns
DIODE C	HARACTERISTICS				 	
V_{SD}	Diode Forward Voltage	I _{SD} = 8 A, V _{GS} = 0 V		0.8	1.0	V
Q _{rr}	Reverse Recovery Charge	V _{DS} = 15 V, I _F = 8 A,		3.4		nC
t _{rr}	Reverse Recovery Time	di/dt = 300 A/µs		5		ns

5.2 Thermal Information

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

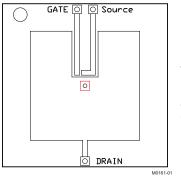
	THERMAL METRIC	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance (1)			5.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ⁽¹⁾⁽²⁾			60	C/VV

⁽¹⁾ R_{θJC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch x 1.5-inch (3.81-cm x 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.

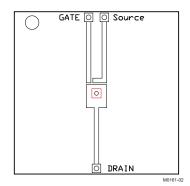
(2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.

Product Folder Links: CSD17579Q3A





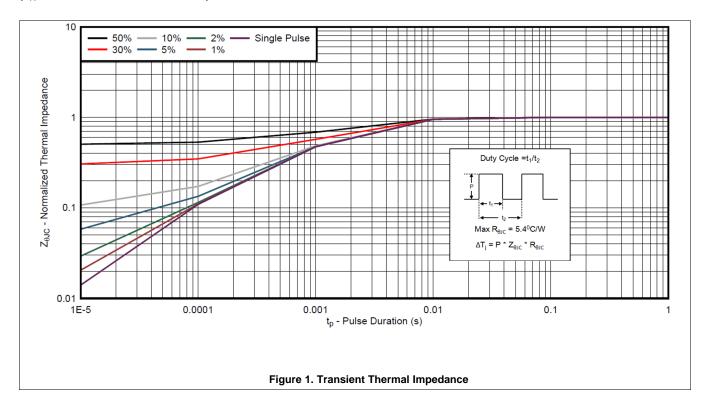
Max $R_{\theta JA} = 60^{\circ}\text{C/W}$ when mounted on 1 inch² (6.45 cm²) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA} = 145^{\circ} C/W$ when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)



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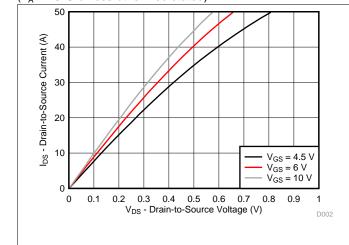
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Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)



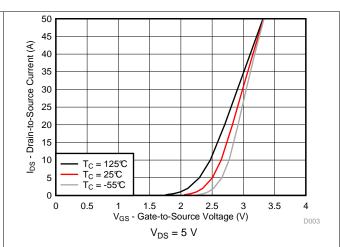
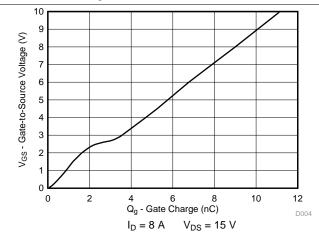


Figure 2. Saturation Characteristics





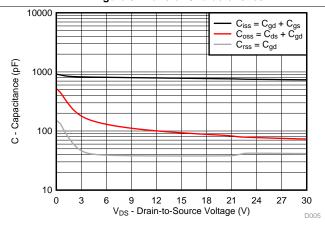


Figure 4. Gate Charge

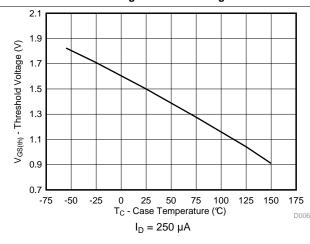


Figure 6. Threshold Voltage vs Temperature

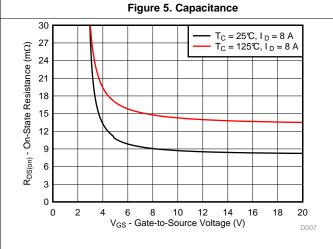


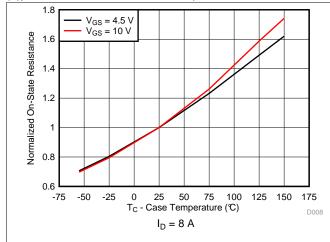
Figure 7. On-State Resistance vs Gate-to-Source Voltage

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Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)



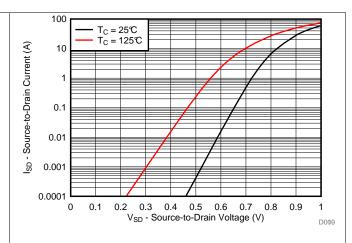
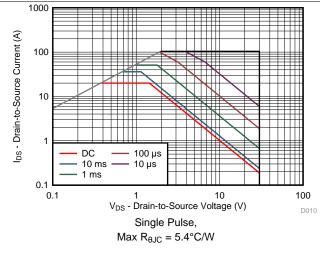


Figure 8. Normalized On-State Resistance vs Temperature

Figure 9. Typical Diode Forward Voltage



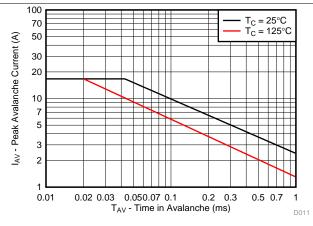


Figure 10. Maximum Safe Operating Area

Figure 11. Single Pulse Unclamped Inductive Switching

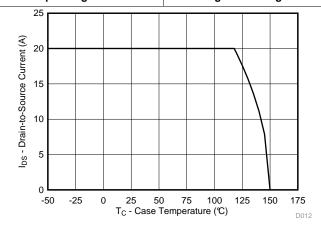


Figure 12. Maximum Drain Current vs Temperature



6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

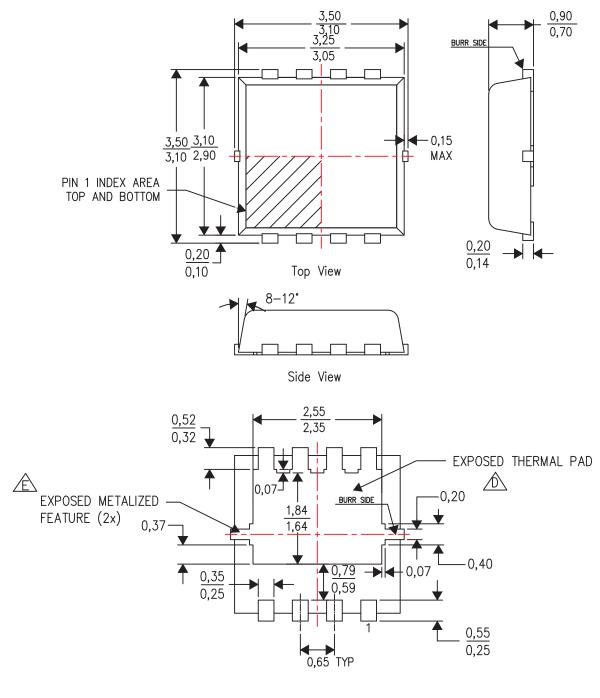
Product Folder Links: CSD17579Q3A

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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

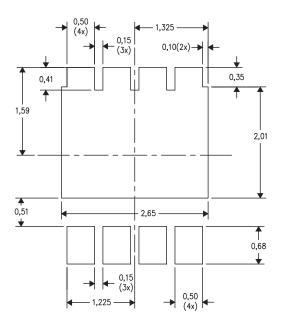
7.1 Q3A Package Dimensions



Bottom View

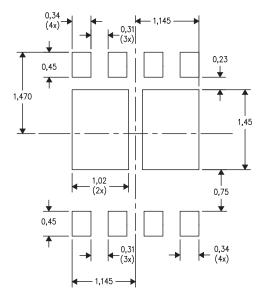


7.2 Q3A Recommended PCB Pattern



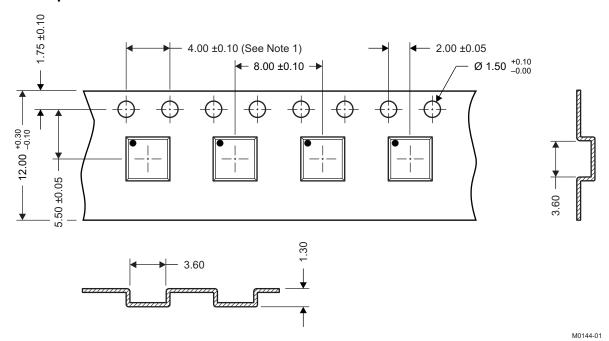
For recommended circuit layout for PCB designs, see application note SLPA005 – Reducing Ringing Through PCB Layout Techniques.

7.3 Q3A Recommended Stencil Pattern



TEXAS INSTRUMENTS

7.4 Q3A Tape and Reel Information



Notes: 1. 10-sprocket hole-pitch cumulative tolerance ±0.2

- 2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
- 3. Material: black static-dissipative polystyrene
- 4. All dimensions are in mm, unless otherwise specified.
- 5. Thickness: $0.30 \pm 0.05 \text{ mm}$
- 6. MSL1 260°C (IR and convection) PbF-reflow compatible



PACKAGE OPTION ADDENDUM

25-Sep-2014

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	_		Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
CSD17579Q3A	PREVIEW	VSONP	DNH	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		17579	
CSD17579Q3AT	PREVIEW	VSONP	DNH	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		17579	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

25-Sep-2014

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